REMARKS

Claims 2-4, 7, 10-13, 15, 18, 20-22 and 25-39 are pending.

I. FORMAL MATTERS

Applicant notes with appreciation that the Examiner has found claim 37 to be allowable if rewritten in independent form.

The Office Action does not acknowledge the claim to priority and does not indicate whether copies of the priority documents have been received. Applicant respectfully requests the Examiner to do so.

Applicant notes with appreciation that the Office Action includes a copy of the PTO Form 1449's that were submitted with the filing of the Divisional Application on March 24, 2004. Each of the references is initialed by the Examiner, thereby indicating that these references were considered.

The Office Action does not indicate whether the drawings filed on March 24, 2004 are acceptable. Applicant respectfully requests the Examiner to do so.

II. REJECTION OF CLAIMS UNDER 35 U.S.C. 112, SECOND PARAGRAPH

Claims 10-13 and 25-28 are rejected under 35 U.S.C. § 112, second paragraph because claims 10 and 25 depend on cancelled claims 1 and 14. Applicant has amended claim 10 to be dependent on claim 29, and claim 25 to be dependent on claim 34.

Also, the Examiner asserts that there is no antecedent basis for "the input switching element" in claims 35 and 38. Regarding claim 35, Applicant has amended claim 35 to recite "an input switching element." Regarding claim 38, this claim does not include this element ("the input switching element").

Based on the foregoing, Applicant submits that this rejection is overcome.

III. PRIOR ART REJECTIONS

A. Claims 2-4, 7, 15, 18, 20-22 and 29-39

Claims 2-4, 7, 15, 18, 20-22 and 29-39 are rejected on the ground of non-statutory obviousness-type double patenting as being unpatentable over claims 1-28 of U.S. Patent No. 6,724,361, which is the parent application (U.S. Application No. 09/703,918).

Applicant submits herewith a Terminal Disclaimer signed by the attorney of record. Thus, Applicant submits that this rejection is overcome.

B. Claims 2-4, 7 and 29-33

Claims 2-4, 7 and 29-33 are rejected under 35 U.S.C. § 103(a) as being unpatentable over applicant's admitted prior art (i.e., Figs. 32-40) in view of U.S. Patent No. 5,128,974 (Maekawa). This rejection is traversed.

The Examiner admits that the admitted prior art does not teach or suggest the switching means of a plurality of stages and asserts that Maekawa discloses: (1) a shift register comprising switching means of a plurality of stages; (2) and a clock signal inputted to the switching means; and (3) that the switching means is added to the shift register to reduce power consumption. The Examiner further asserts that it would have been obvious to use Maekawa's switching means in the shift register of the admitted prior art in order to reduce power consumption.

Applicant submits that the Examiner has not set forth a prima facie case of obviousness. In order to establish a prima facie case of obviousness, the relied upon prior art must teach all of the claim limitations (see MPEP § 2142). Applicant submits that Maekawa does not teach or suggest all the features of claim 29, such as "the switching means on each of the stages is such that an input of a clock signal is controlled by the flip-flop on an immediately preceding stage controlling an open/closed state of that switching means through an output signal from that flip-flop; and a clock signal inputted to the switching

means which is ON is a set input to the flip-flop on an immediately succeeding stage and an output pulse from that succeeding stage in the shift register," on which claims 2-4, 7 and 28-33 depend. Therefore, Applicant submits that the Examiner has not set forth a prima facie case of obviousness. Applicant respectfully requests the Examiner to cite a prior art reference that teaches these features of claim 29, or withdraw the rejection.

With the arrangement "a clock signal (as it is) inputted to the switching means is an output pulse from that succeeding stage in the shift register," and output pulses with no overlapping can be obtained without using a complicated circuit including a logic element or the like, because the close signals pass through the switching without any significant delay (see page 37, lines 12 to 22 of the present specification of the present Application).

On the other hand, Maekawa has such an arrangement that the clock signal (VCLK, VCLK) is inputted to the unit register (SR) including a logic element such as an inverter (INV1, INV2), after passing a switch (SW1, SW2). Thus the output of the unit register (SR) is the output of the shift register. That is, the clock signal (as it is) is not the output pulse of the shift register in Maekawa.

C. Claims 15, 18, 20-22, and 34-36

Claims 15, 18, 20-22, and 34-36 are rejected under 35 U.S.C. § 102(e) as being anticipated by Ishii (U.S. Patent No. 6,670,944). This rejection is traversed.

The Examiner asserts that column 11, lines 17-30 and 62-67 and Figs. 4, 9 and 12 disclose the features of claim 34. This section if Ishii discloses a shift register circuit 1560 that includes n unit circuits connected in cascade fashion. Level shifters 1510 and 1520 are disposed at locations corresponding to the unit circuits at respective stages of the shift register circuit 1560. Ishii teaches that the level shifters 1510 and 1520 receive a signal output from a latch circuit 1530, and the set input S of the latch circuit 1530 is coupled to the output of the level shifter located immediately before the certain level shifter (see column 11, line 62 – column 12, line 4). This section of Ishii does not teach the feature of claim 34 (i.e., each of the level shifters is such that a clock signal voltage raising operation thereof is controlled by the flip-flop on an immediately preceding stage to that level shifter through an output signal from that flip-flop; and the clock signal voltage-raised by that level shifter is an input to the flip-flop on an immediately succeeding stage and an output pulse from that succeeding stage in the shift register). Because Ishii does not teach each and every feature of claim 34, on which claims 15, 18, 20-22, and 35-36 depend, Ishii does not anticipate claims 15, 18, 20-22, and 34-36. Thus, the rejection of claims 15, 18, 20-22, and 34-36 under 35 U.S.C. § 102(e) is improper and should be withdrawn.

The output signal from the latch circuit of Ishii (1530) is inputted to the level shifter (1510, 1520), and the set input S of the latch circuit is connected to the output of the level shifter immediately preceding that latch circuit. That is, Ishii does not disclose the arrangement of Claim 34. More specifically, Ishii does not disclose the arrangement "each of the level shifters is such that a clock signal voltage raising operation thereof is controlled by the flip-flop on an immediately preceding stage to that level shifter through an output signal from that flip-flop; and the clock signal voltage-raised by the level shifter is an input to the flip-flop on an immediately succeeding stage and an output pulse from that succeeding stage in the shift register."

In addition, the element "the clock signal voltage-raised by the level shifter is an output pulse from that succeeding stage in the shift register" is not disclosed in Ishii. That is, Ishii is arranged such that the clock signal whose voltage is increased by the shift register is outputted via the shift register (1560), but the shift register (1560) is a complicated circuit including a logic element as illustrated in FIG. 7. Thus, the clock signal (as it is) is not the output pulse of the shift register in Ishii."

D. Claims 38-39

Claims 38-39 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Ishii. This rejection is traversed.

As presented above, Ishii fails to disclose several important features of claim 34, on which claims 38-39 depend. Therefore, the rejection of claims 38-39 under 35 U.S.C. § 103(a) is improper and should be withdrawn.

Therefore, based on the foregoing, Applicant submits that the present application is in condition for allowance and allowance is respectfully solicited.

If the Examiner believes that any outstanding issue could be resolved through a telephone interview, Applicant kindly requests the Examiner to contact the undersigned at the telephone number listed below.

Applicant believes that no additional fees are due for the subject application. However, if for any reason a fee is required, a fee paid is inadequate or credit is owed for any excess fee paid, you are hereby authorized and requested to charge Deposit Account No. **04-1105**.

Respectfully Submitted,

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